Turn-Around Phenomenon in the Degradation Trend of n-Type Low-Temperature Polycrystalline Silicon Thin-Film Transistors under DC Bias Stress

Han-Wen Liu*, Si-Ming Chiou, and Fang-Hsing Wang

Department of Electrical Engineering and Institute of Electrical Engineering, and Graduate Institute of Optoelectric Engineering, National Chung Hsing University, Taichung 402, Taiwan, R.O.C.

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In this research, the instability of n-type low-temperature polycrystalline silicon (poly-Si) thin-film transistors (LTPS TFTs) is investigated under DC bias stress and a unique phenomenon is observed. At a large gate stressing voltage and simultaneous low to moderate drain biasing voltages operating in a linear region, a turn-around phenomenon is observed in the on-current (I_{on}) degradation trend of the TFT characteristics, resulting from the increase in maximum transconductance ($G_{m,max}$). However, under a larger drain stressing voltage, the turn-around phenomenon of the I_{on} degradation trend is observed to disappear owing to the extensive increases in threshold voltage (V_{th}) and trap state density (N_{trap}) in a channel, which cause the TFTs to deteriorate monotonically. © 2010 The Japan Society of Applied Physics

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1. Introduction

Low-temperature polycrystalline silicon (poly-Si) thin-film transistors (LTPS TFTs) have attracted considerable attention in flat-panel displays (FPDs), such as an active matrix liquid crystal display (AMLCD) and an active matrix organic light-emitting diode (AMOLED). Both the pixel switching element in the panel and peripheral driving circuits could be integrated into the same substrate owing to the high driving capability of LTPS TFTs. However, the degradation characteristic of the devices is an important issue in the applications mentioned above.

It is well known that the threshold voltage and mobility of the LTPS TFTs degrade via two main mechanisms, i.e., hot carrier and self-heating effects. Previous studies revealed that the hot carrier effect is caused by a high drain field around the drain,[1–5] typically at low gate and high drain stressing voltages, and could be suppressed by a lightly doped drain (LDD) structure.[1] On the other hand, the self-heating effect degrades devices with defect states at the interface and poly-Si channel owing to the breaking of Si–H bonds and the regeneration of dangling bonds.[2] The self-heating effect is also called the Joule heating effect caused by a high drain current,[4–7] generally at high gate and high drain stressing voltages, owing to the low thermal conductivity of the glass substrate. The accumulated heat breaks weak Si–H bonds and generates deep-state defects.

By considering different gate and drain stressing voltages, the hot carrier and self-heating effects located in different regions of the diagram for stressing drain-/gate-voltage-dependent parameters and the instability of on-/off-current have been studied.[2,5] However, these studies are focused on either the hot carrier effect or the self-heating effect, and there are very few studies[8] that investigated beyond these two regions, that is, LTPS TFTs suffer from DC bias stress at low gate and high drain stressing voltages for the hot carrier effect, and at both high gate and drain stressing voltages for the self-heating effect. In this study, we investigate the instability of n-type LTPS TFTs stressed with a fixed high gate voltage and different drain voltages. Moreover, a special turn-around phenomenon in the on-current (I_{on}) degradation trend is observed and a defect state generation model is proposed to explain this phenomenon.

*E-mail address: hwliu@dragon.nchu.edu.tw

2. Experimental Procedure

The n-channel LDD TFTs used in this study have a channel width of 20 µm and a channel length of 5 µm. The process flow of TFTs is described as follows. First, a buffer oxide layer and a 50-nm-thick hydrogenated amorphous silicon (a-Si:H) thin film are deposited by plasma-enhanced chemical vapor deposition (PECVD) on a glass substrate. The samples are then dehydrogenated in nitrogen (N_2) ambient. A XeCl excimer laser of 308 nm wavelength and 400 mJ/cm^2 energy density is applied to recrystallize an a-Si film to poly-Si. After active region patterning, a 100-nm-thick tetraethoxysilane (TEOS) gate oxide layer is deposited by PECVD. Next, a metal gate is formed by sputtering and then a pattern is defined. The LDD structure is fabricated by $^{31}P^+$ self-aligned implantation at a dosage of 2×10^{13} cm^{-2}, and the n$^+$ source and drain doping is performed by $^{31}P^+$ implantation at a dosage of 5×10^{15} cm^{-2}. The length of the LDD is 1.5 µm. Then, a 500-nm-thick SiO_2 layer is deposited by PECVD as the passivation layer. Subsequently, the samples are treated at 600 °C in N_2 ambient for 24 h for dopant activation. Hydrogenation is performed to improve the electrical property of the TFTs. After the contact hole formation and metallization, the samples are treated at 400 °C in N_2 ambient for 30 min to complete the fabrication of TFTs.

In the DC bias stress test, a drain current to gate voltage (I_d–V_g) transfer curve is measured using an Agilent 4156C, and various electrical parameters of the TFTs are extracted from this transfer curve. We apply bias stress to the gate and drain simultaneously. The gate bias (V_g) is +18 V and the drain biases (V_d) are +3, +6, +9, +12, and +15 V; the source is grounded. An abnormal curve is observed at a +9 V drain bias. For detailed observation, the same experiments with extra bias conditions and a much longer stress time are carried out. The gate bias is also kept at +18 V and the drain biases are +6, +7.5, +9, and +10.5 V; the source is grounded. On-current (I_{on}) is defined as the drain current (I_d) corresponding to $V_g = +10$ V and $V_d = +0.1$ V. The degradation of I_{on} is defined as $\Delta I_{on}/I_{on,0}$, where $I_{on,0}$ is the initial on-current and ΔI_{on} is the difference between $I_{on,stress}$ (on-current after stress) and $I_{on,0}$. Moreover, the transconductance (G_m) is derived by differentiating drain current with respect to gate voltage in the linear region operation. We examine the degradation of maximum

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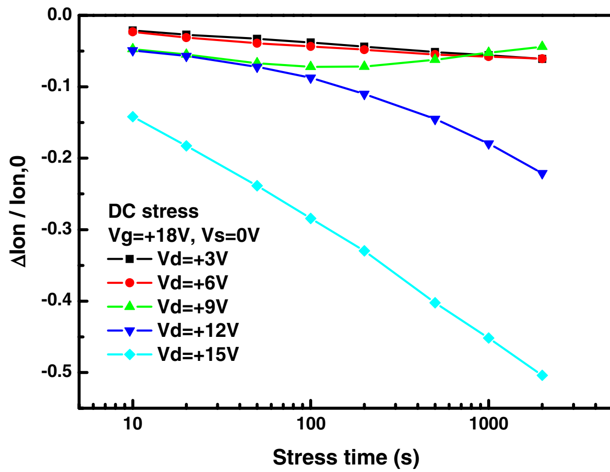

Fig. 1. (Color online) Degradation characteristics of I_{on} with fixed gate and different drain stressing voltages.

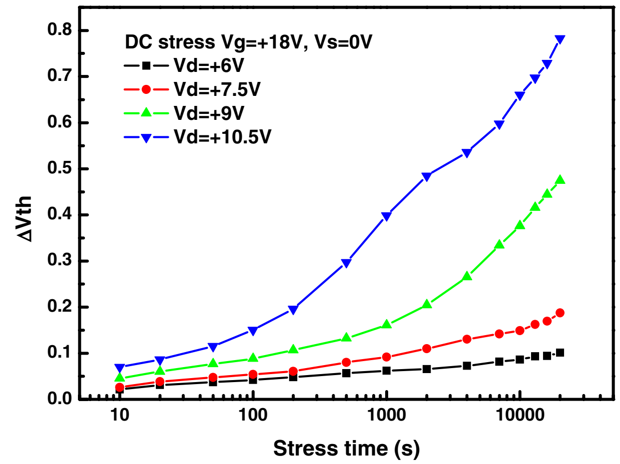

Fig. 3. (Color online) Degradation trend of V_{th} with moderate drain stressing voltages.

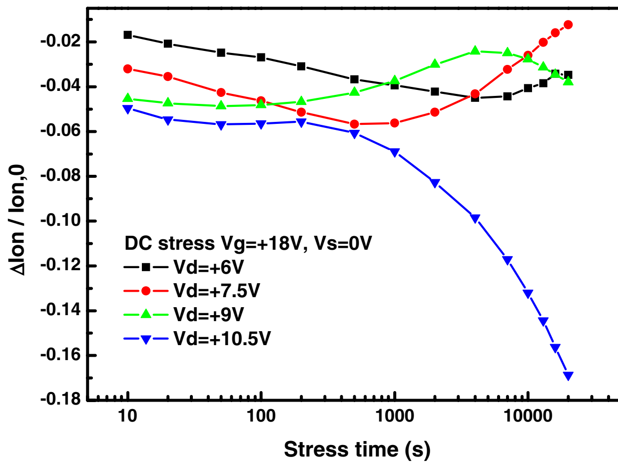

Fig. 2. (Color online) Turn-around phenomena in the degradation trend of I_{on} with moderate drain stressing voltages.

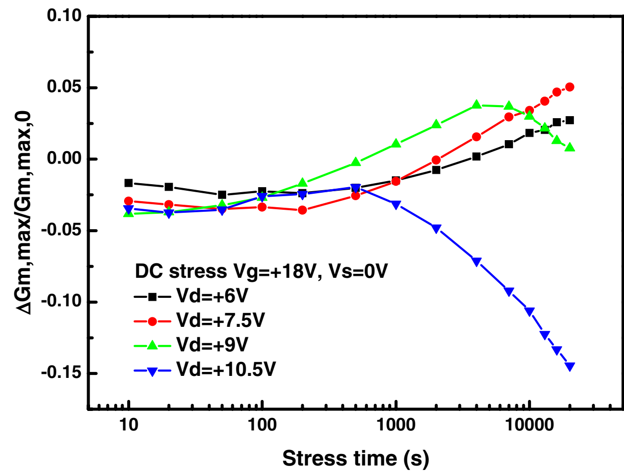

Fig. 4. (Color online) Turn-around phenomena in the degradation trend of $G_{m,max}$ with moderate drain stressing voltages.

transconductance ($G_{m,max}$) using $\Delta G_{m,max}/G_{m,max,0}$, where $G_{m,max,0}$ is the initial $G_{m,max}$ and $\Delta G_{m,max}$ is the difference between $G_{m,max,stress}$ ($G_{m,max}$ after stress) and $G_{m,max,0}$. Moreover, threshold voltage (V_{th}) is defined as the V_g corresponding to the $I_d = (W/L) \times 10\,\text{nA}$ at $V_d = +0.1\,\text{V}$.

3. Results and Discussion

Figure 1 shows the degradation curves of I_{on} at a fixed gate bias (+18 V) for different drain stressing voltages. The degradation increases as drain stressing voltage increases.[6] For most cases, the degradation increases with stress time, except at $V_d = +9\,\text{V}$, where the degradation curve turns up, and a noticeable turn-around phenomenon is observed. To confirm that this turn-around phenomenon is not a single event, repeated experiments are carried out with drain stressing voltages of approximately +9 V and a longer stress time of up to 20000 s. Figures 2–4 show the time-dependent degradation trends of I_{on}, V_{th}, and $G_{m,max}$, respectively, after applying DC bias stress. The degradations of all the electrical characteristics are not severe owing to the LDD structure of TFTs. In Fig. 2, it is observed that the larger the drain stressing voltage is, the earlier the turn-around phenomenon occurs. The times for the turn-around phenomenon are 20, 50, 500, and 4000 s for drain stressing voltages of +10.5, +9, +7.5, and +6 V, respectively. In particular, in the case of $V_d = +9\,\text{V}$, the degradation curve goes down again when the stress time is sufficiently long. Figure 3 shows the degradation curves for V_{th} with drain stressing voltages between +6 and +10.5 V, and a fixed gate voltage of +18 V. Because the initial V_{th} of the adopted TFTs is about +1.5 V, the stressing conditions mentioned above enable the TFTs to operate in a linear region. V_{th} increases monotonically when drain voltage and stress time increase; however, no turn-around phenomenon is observed in the degradation curves. Therefore, the turn-around phenomenon of I_{on} degradation is not only directly related to threshold voltage degradation but also to other causes. However, as shown in Fig. 4, a similar turn-around phenomenon in $G_{m,max}$ degradation is observed at lower drain stressing voltages. When the drain stressing voltage is smaller than +9 V, the $G_{m,max}$ degradation values even become positive at a very long stress time. This means that the field-effect mobility of electrons in n-type LTPS TFTs increases with increasing stress time. It is conjectured that I_{on} degradation is affected by the combination of the degradations of $G_{m,max}$ and V_{th} under DC bias stress, but the degradation of $G_{m,max}$ is dominant in the first turn-around

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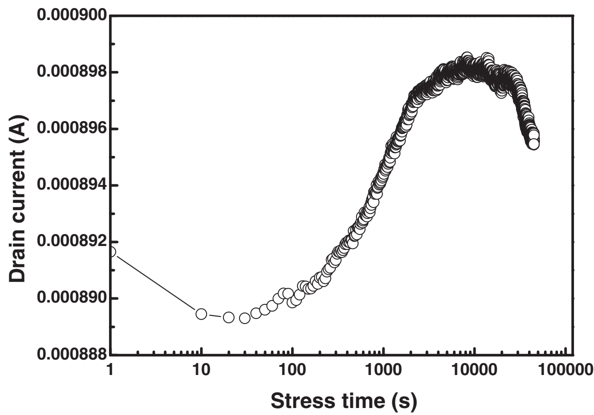


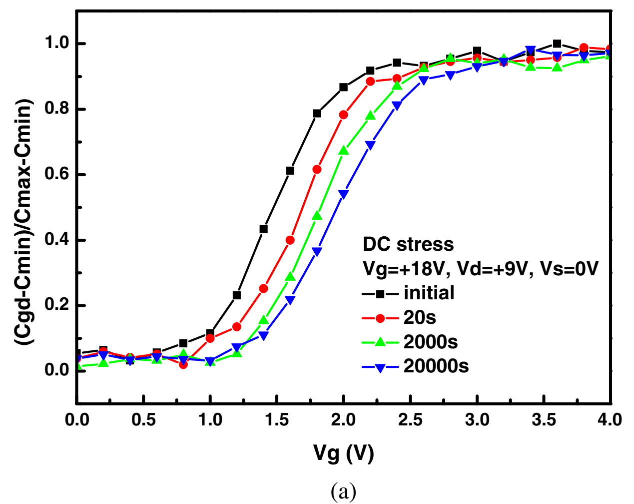
Fig. 5. Time dependence of sampling current I_d with stressing voltages of $V_g = +18$ V and $V_d = +9$ V.

period. Figure 5 shows the time-dependent sampling current I_d (drain current) with stressing voltages of $V_g = +18$ V and $V_d = +9$ V, which is simultaneously measured using an Agilent 4156C under DC bias stress. There are two notable turn-around points in the sampling current I_d curve coinciding with the degradation trends of I_{on} and $G_{m,max}$, shown in Figs. 2 and 4, respectively.

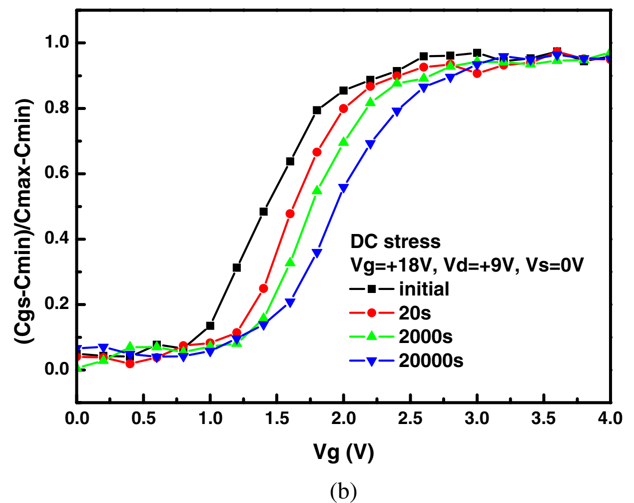
Figure 6 shows the time-dependent C–V curves under the stress conditions of $V_g = +18$ V and $V_d = +9$ V, which are measured at a frequency of 1 MHz. The curves of the capacitances C_{gd} (between the gate and the drain with source floating) and C_{gs} (between the gate and the source with drain floating) are almost the same and show no change in shape; they only shift forward to the positive direction, which coincides with the degradation of V_{th}, as shown in Fig. 3. The behavior trends of these C–V curves showing no stretching out cannot be explained by the hot carrier effect.[3,7] Furthermore, no increase in capacitance below the flatband voltage (V_{FB}) is observed in our C–V curves indicating the absence of the self-heating effect in the stress test of $V_g = +18$ V and $V_d = +9$ V.[7]

Figure 7 shows the time-dependent trap state density after applying DC bias stress with a fixed gate and different drain stressing voltages. The trap state density (N_{trap}, cm^{-2}) is calculated from the square root of the slope of the $\ln(I_D V_{DS}/V_{GS})$ vs $1/V_{GS}{}^2$ plots, which was proposed by Proano *et al.*[9] The higher the drain stressing voltage is, the higher the trap state density becomes. N_{trap} increases monotonically when drain voltage and stress time increase, and no turn-around phenomenon is observed in the curves. When the drain stressing voltages are low to moderate, N_{trap} increases slowly with increasing stress time in the early stage. Therefore, there is a turn-around phenomenon of I_{on} degradation in this period, resulting from the increase in $G_{m,max}$. On the other hand, as drain stressing voltage increases toward a sufficiently large value (+12 V or over, in this study), N_{trap} increases rapidly and then predominates the degradation from the very beginning, causing a monotonic I_{on} degradation, as shown in Fig. 1.

For the unusual turn-around phenomena of I_{on} degradation observed in this research, we propose a defect state generation model to explain them. Since the initial V_{th} of the adopted TFTs is about +1.5 V, the stressing conditions of high gate and low drain voltages will enable the TFTs to operate in the linear region. Figure 8 shows the demonstrated schematic diagram for the generation of defect states. First, in the early stressing period, I_{on} decreases, owing to the trapping of a few electrons in the gate insulator and the trap state



(a)



(b)

Fig. 6. (Color online) Time dependence of capacitance vs voltage curves with stressing voltages of $V_g = +18$ V and $V_d = +9$ V. (a) C_{gd} and (b) C_{gs}.

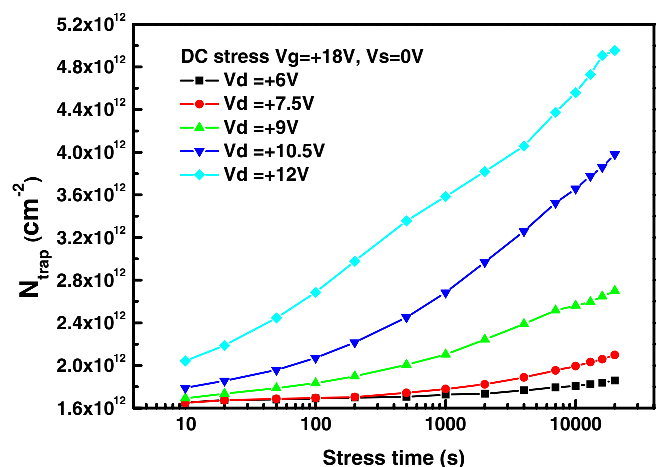


Fig. 7. (Color online) Time dependence of trap state density, N_{trap}, after DC bias stress with fixed gate and different drain stressing voltages.

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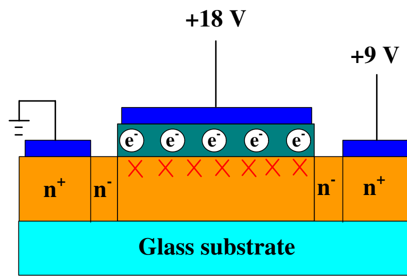

Fig. 8. (Color online) Proposed defect state generation model of the LTPS TFTs under DC stress conditions of $V_g = +18\,V$, $V_d = +9\,V$, and source grounded; "X" denotes the trap state defects in the channel.

generation in the poly-Si film. These defects cause a V_{th} increase and an I_{on} decrease. As stress time increases, I_{on} increases owing to the increase in $G_{m,max}$, as shown in Fig. 4. However, the mechanism of the increase in $G_{m,max}$ in this period needs to be studied thoroughly. Finally, as stressing time becomes sufficiently long, the number of trapped electrons in the gate oxide and the channel trap state defect density increase extensively, which causes a V_{th} increase and a $G_{m,max}$ decrease. Therefore, I_{on} decreases again.

4. Conclusions

In this research, we study the I_{on} degradation of n-channel LTPS TFTs under DC bias stress. At a large gate stressing voltage, V_g, and simultaneous low to moderate drain biasing voltages, a turn-around phenomenon is observed in the degradation trend of the TFT characteristics, such as I_{on} and $G_{m,max}$. This phenomenon cannot be ascribed to the hot carrier effect or explained by the self-heating effect. A defect state generation model is proposed to explain this turn-around phenomenon.

Because the V_{th} and N_{trap} increase monotonically and slightly with stress time under high gate and low to moderate drain stressing voltages, the turn-around phenomenon of I_{on} degradation is mainly caused by the variation in $G_{m,max}$. As the drain stressing voltage is sufficiently large, the turn-around phenomenon will disappear owing to the extensive increases in V_{th} and N_{trap}. In this study, under the $V_g = +18\,V$ stressing condition, an evident turn-around phenomenon of the degradation is observed at approximately $V_d = +9\,V$, whereas only a monotonic deterioration of TFTs is observed at V_d of over $+12\,V$.

Acknowledgements

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